

This is an examiner's amendment.

A dual residue pipelined AD converter

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8/1/07 { This application is a 371 of PCT/IB04/52129, which has an international filing date of October 18, 2004, designating the United States of America, and claims the benefit of European Patent application 03103935.7 Filed October, 23, 2003.

The invention relates to a dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising a cascade of dual residue converter stages, the first of said stages comprising means to receive the analog input signal, means to derive one or more digital bits from said analog input signal and means to generate first and second residue signals representing the quantization error left after the AD-conversion of said first stage, each of the following stages in the cascade of dual residue converter stages comprising means to receive the first and second residue signals generated by the previous stage in the cascade, means to derive one or more further digital bits from said received first and second residue signals and each of said following stages except the last one in the cascade comprising means to generate first and second residue signals representing the quantization error left after the AD-conversion of the stage. Such dual residue pipelined AD converter is known from the paper "A Two Residue Architecture for Multistage ADC's" by Mangelsdorf et al, 1993 IEEE International Solid State Circuits Conference, February 24, 1993.

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A single residue pipelined AD converter comprises a plurality of cascaded stages of which each stage calculates only a part (k) of the bits of the desired total digital word. To this end the stage contains a k-bit AD converter that compares the analog input with at least one reference voltage and that outputs a k-bit digital signal resulting from this comparison. Subsequently a residue signal is derived. This derivation may be considered as applying the k-bit digital output of the AD converter to a DAC that delivers the analog representation of this k-bit signal and generating the difference between the analog input and the analog representation of the k-bit signal. This difference is the quantization error or residue that is applied to the next stage of the cascade for deriving the next bit(s) of the digital word. A major drawback of such single residue pipelined AD converter is that the residue signal, prior to being applied to the next stage of the cascade, has to be amplified with a factor that is very closely equal to 2^k . This not only in order to optimally use the dynamic range of the next stage but, more importantly, to be able to use the derived reference